IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Hanna, S.

SERIAL NO. 09/879,589 EXAMINER: Unassigned

FILED: July 12, 2001 ART UNIT: Unassigned

TITLE: TIMER/TIMEOUT EVALUATION SYSTEM

Attorney Docket No.: BLD920000046US1

Commissioner For Patents
Washington, D.C. 20231

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on OCT 5, 2001 (Date of Deposit)

VICTORIA E. ROESER
Name

Victoria E. Roeser
Signature

PRELIMINARY AMENDMENT

Dear Sir:

Before prosecution, please amend the application as follows:

In the Specification

On page 3, please amend line 10 as follows:

Figures 3a and 3b show block diagrams of the timeout evaluation circuitry of Figure 2; and

On page 4, please amend the paragraph beginning on line 25, and ending on line 30, as follows:

Figures 3a and 3b show the components of the timeout evaluation circuitry 40. The components include a clock circuit 52, a state machine 65 for setting initial conditions that enable the clock circuit 52, a 16 bit compare circuit 70, also for setting initial conditions that enable the clock circuit 52, and at least one timeout unit 80a-80h for evaluating timers or timeout conditions as represented by signals 15a-15h.

On page 6, please amend the paragraph beginning on line 9, and ending on line 22, as follows:

The timeout evaluation circuitry 40 further includes at least one timer unit. Figure 3a shows a preferred embodiment that comprises eight timer units, 80a-80h. The timer units serve as timers to time certain events in the printer 200 by monitoring signals associated with those events. Because the structure of each timer unit is the same, only the structure of timer unit 80a will be described. The timer unit 80a is comprised of an 8 bit timeout counter 85a that has as its inputs the incrementing signal (INCR_NEW_OBJ 20a) and the corresponding signal being evaluated (RESET_NEW_OBJ 15a). The output of the 8 bit counter 85a is coupled to an 8 bit compare circuit 90a and to an 8 bit latch and hold register 95a. The output of the 8 bit compare circuit 90a is coupled to the 8 bit latch and hold register 95a and loads the output value of the 8 bit counter 85a into the 8 bit latch and hold register 95a if the output value of 85a exceeds the value currently stored in the 8 bit latch and hold register 95a. The 8 bit latch and hold register 95a is initialized to a value of 00 when the Start_Print signal 45a equals 0.

On page 6, please amend the paragraph beginning on line 28, and ending on line 29, as follows:

The operation of the timeout evaluation system 10 will now be described with reference to Figures 3a, 3b, and 4.

On page 7, please amend the paragraph beginning on line 21, and ending on line 28, as follows:

Also upon initialization, the 10 bit counter 55 begins counting, driven by the 16 MHz Clock signal 45d. The output of the 10 bit compare circuit 60 is suppressed until the initial conditions determined by the state machine 65 and the 16 bit compare circuit 70 are satisfied. As shown in Figure 3b, the initial conditions include the output of the state machine 65 reaching 11 for the first time and the output of the 16 bit compare circuit 70 becoming active. The output of the 10 bit compare circuit 60 may also be suppressed by other "non initial" conditions, for example, when signal T_ADDR 45c is less than or equal to 002F.

Please amend the paragraph beginning on page 7, line 27, and ending on page 9, line 11, as follows:

Incrementing signal 20a increments 8 bit counter 85a, while signal 15a resets 8 bit counter 85a each time it equals "1," thus starting another timing cycle. The 8 bit compare circuit 90a loads the output of the 8 bit counter 85a into the 8 bit latch and hold circuit 95a if the value of the output of the 8 bit counter 85a is greater than the value held in the 8 bit latch and hold circuit 95a (steps 445 and 450. Figure 4). Thus, the 8 bit latch and hold circuit 95a holds the maximum count achieved by the counter over multiple counting cycles. The outputs of the 8 bit latch and hold circuits 95a-95h are coupled to an 8 bit compare circuit 100. If any of the outputs reaches a predetermined count before being reset, in this embodiment preferably FF, the 8 bit compare circuit 100 generates a signal Timeout_EQ_FF which latches the outputs of all the latch and hold circuits 95a-95h, as shown in steps 445 and 450 of Figure 4B. The printer 200 is able to read the latched outputs of the 8 bit latch and hold circuits 95a-95h through the data mux 50 by using signals 45f and 45g.

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REMARKS

Claims 1-12 remain in the application.

Upon conversion of the informal drawings to formal drawings, the information originally included on Figure 3 was required to be split between Figures 3a and 3b. References to Figure 3 in the specification have been amended accordingly.

The paragraph on page 7, beginning on line 27, has been amended to correct typographical errors.

Attached hereto is a marked up version of the changes made to the specification by the current amendment. The attached page is captioned "Version With Markings to Show Changes Made."

Respectfully submitted,

10/5/01
Date

Paul D. Greeley
Attorney for Applicant
Registration No. 31,019
Ohlandt, Greeley, Ruggiero & Perle, L.L.P.
One Landmark Square, 10th Floor
Stamford, CT 06901-2682
(203) 327-4500

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification

On page 3, please amend line 10 as follows:

[Figure 3 is a] Figures 3a and 3b show block [diagram] diagrams of the timeout evaluation circuitry of Figure 2; and

On page 4, please amend the paragraph beginning on line 25, and ending on line 30, as follows:

[Figure 3 shows] Figures 3a and 3b show the components of the timeout evaluation circuitry 40. The components include a clock circuit 52, a state machine 65 for setting initial conditions that enable the clock circuit 52, a 16 bit compare circuit 70, also for setting initial conditions that enable the clock circuit 52, and at least one timeout unit 80a-80h for evaluating timers or timeout conditions as represented by signals 15a-15h.

On page 6, please amend the paragraph beginning on line 9, and ending on line 22, as follows:

The timeout evaluation circuitry 40 further includes at least one timer unit. Figure [3] 3a shows a preferred embodiment that comprises eight timer units, 80a-80h. The timer units serve as timers to time certain events in the printer 200 by monitoring signals associated with those events. Because the structure of each timer unit is the same, only the structure of timer unit 80a will be described. The timer unit 80a is comprised of an 8 bit timeout counter 85a that has as its inputs the incrementing signal (INCR_NEW_OBJ 20a) and the corresponding signal being evaluated (RESET_NEW_OBJ 15a). The output of the 8 bit counter 85a is coupled to an 8 bit compare circuit 90a and to an 8 bit latch and hold register 95a. The output of the 8 bit compare circuit 90a is coupled to the 8 bit latch and hold register 95a and loads the output value of the 8 bit counter 85a into the 8 bit latch and hold register 95a if the output value of 85a exceeds the value currently stored in the 8 bit latch and hold register 95a. The 8 bit latch and hold register 95a is initialized to a value of 00 when the Start_Print signal 45a equals 0.

On page 6, please amend the paragraph beginning on line 28, and ending on line 29, as follows:

The operation of the timeout evaluation system 10 will now be described with reference to Figures [3] 3a, 3b, and 4.

On page 7, please amend the paragraph beginning on line 21, and ending on line 28, as follows:

Also upon initialization, the 10 bit counter 55 begins counting, driven by the 16 MHz Clock signal 45d. The output of the 10 bit compare circuit 60 is suppressed until the initial conditions determined by the state machine 65 and the 16 bit compare circuit 70 are satisfied. As shown in Figure [3] 3b, the initial conditions include the output of the state machine 65 reaching 11 for the first time and the output of the 16 bit compare circuit 70 becoming active. The output of the 10 bit compare circuit 60 may also be suppressed by other "non initial" conditions, for example, when signal T_ADDR 45c is less than or equal to 002F.

Please amend the paragraph beginning on page 7, line 27, and ending on page 9, line 11, as follows:

Incrementing signal 20a increments 8 bit counter 85a, [(step 425 of Figure 4A)] while signal 15a resets 8 bit counter 85a each time it equals "1," thus starting another timing cycle [as shown in step 430 of Figure 4A]. The 8 bit compare circuit 90a loads the output of the 8 bit counter 85a into the 8 bit latch and hold circuit 95a if the value of the output of the 8 bit counter 85a is greater than the value held in the 8 bit latch and hold circuit 95a (steps [435, Figure 4A and step 440, Figure 4B] 445 and 450, Figure 4). Thus, the 8 bit latch and hold circuit 95a holds the maximum count achieved by the counter over multiple counting cycles. The outputs of the 8 bit latch and hold circuits 95a-95h are coupled to an 8 bit compare circuit 100. If any of the outputs reaches a predetermined count before being reset, in this embodiment preferably FF, the 8 bit compare circuit 100 generates a signal Timeout_EQ_FF which latches the outputs of all the latch and hold circuits 95a-95h, as shown in steps 445 and 450 of Figure 4B. The printer 200 is able to read the latched outputs of the 8 bit latch and hold circuits 95a-95h through the data mux 50 by using signals 45f and 45g.